3100
FIVE-INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3100 dual five-input gate is a MOS monolithic integrated circuit. This device can be utilized as a logic block in an all MOS system, or as a breadboarding gate in designing customer integrated circuits. Input protection is provided on all inputs.

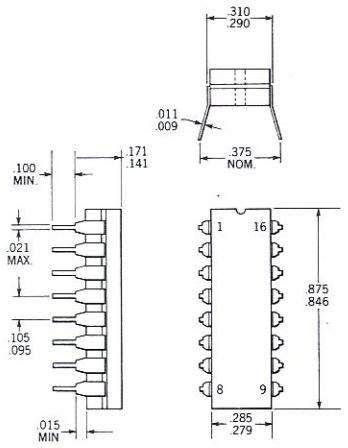
FEATURES

- **GATE PROTECTION**
- **INVERTED AND NON-INVERTED OUTPUT BUFFERS**
- **AND/OR, NAND/NOR CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (Notes 2 & 3)

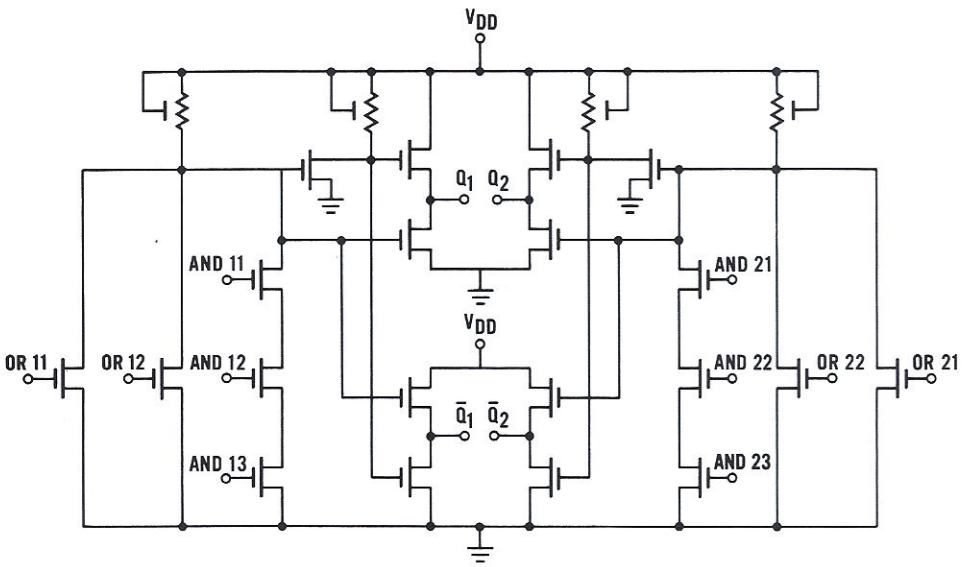
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any pin	−30 V

PHYSICAL DIMENSIONS
16 Lead Dual In-Line

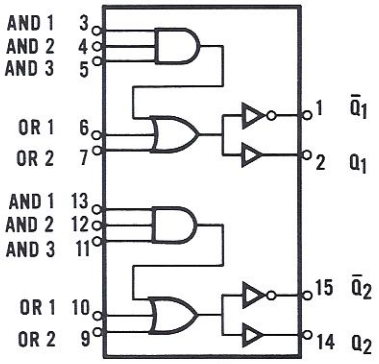


ORDER PART NO. A6J310014X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



GND = 8
V_{DD} = 16

NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:
(1) These ratings are limiting values above which serviceability may be impaired.
(2) Voltage levels are with respect to GND Pin.

Electrical Characteristics on Page 2

*Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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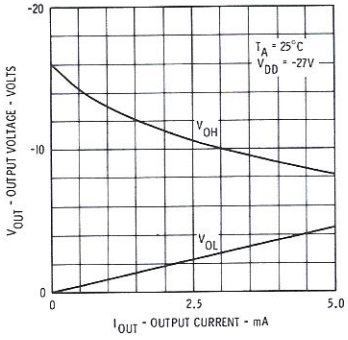
FAIRCHILD MOS INTEGRATED CIRCUIT • 3100

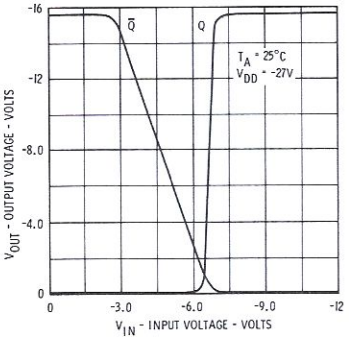
ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, Load = 10 MΩ, 10 pF, $T_A = +25°C$ unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Output Impedance to Ground		1.0	1.5	kΩ	$I_{OUT} = 100\ \mu A$
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	0.5			μs	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{pd+} (Q)		0.4		μs	
t_{pd-} (Q)		0.4		μs	
t_{pd+} ($\overline{Q}$)		0.4		μs	
t_{pd-} ($\overline{Q}$)		0.6		μs	
Power Consumption		60		mW	

TYPICAL OUTPUT CHARACTERISTIC



TYPICAL TRANSFER CHARACTERISTICS



TRUTH TABLE

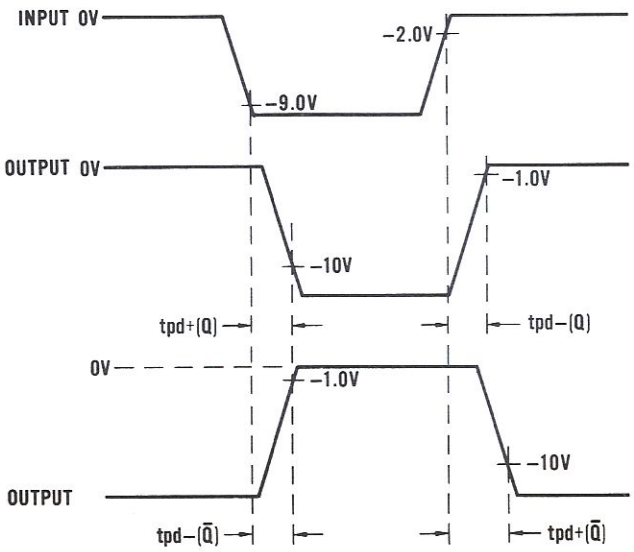
A OR_1	B OR_2	C AND_1	D AND_2	E AND_3	Q	$\overline{Q}$
0	0	0	0	0	0	1
0	0	0	0	1	0	1
0	0	0	1	0	0	1
0	0	0	1	1	0	1
0	0	1	0	0	0	1
0	0	1	0	1	0	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	X	X	X	1	0
1	0	X	X	X	1	0
1	1	X	X	X	1	0

Logical '1' is more negative than −9.0 V
Logical '0' is more positive than −2.0 V and ≤ 0 V
X is either '1' or '0'

BOOLEAN FUNCTION: $Q = \overline{A + B + C \cdot D \cdot E}$

$\overline{Q} = A + B + C \cdot D \cdot E$

TYPICAL PROPAGATION DELAY



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